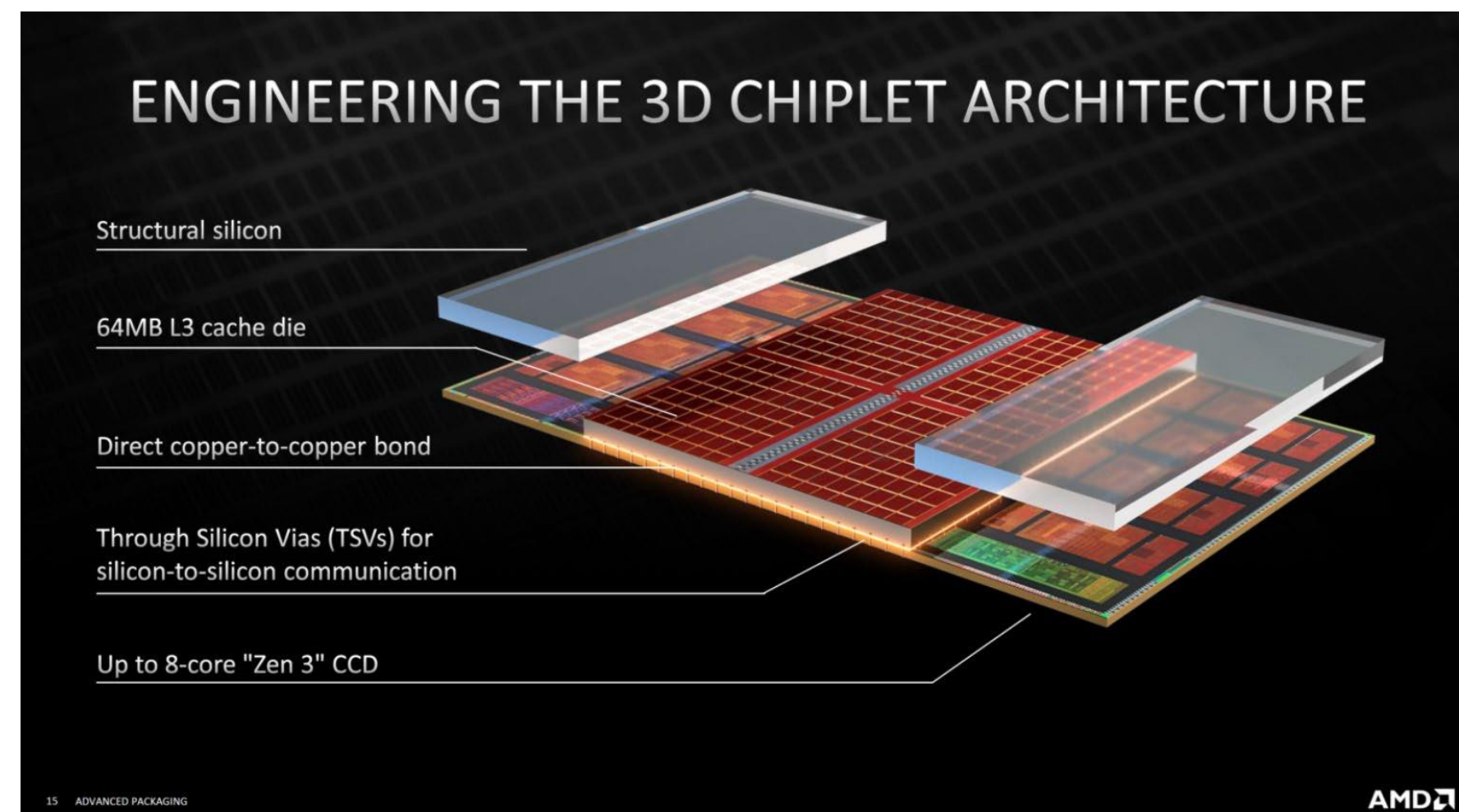
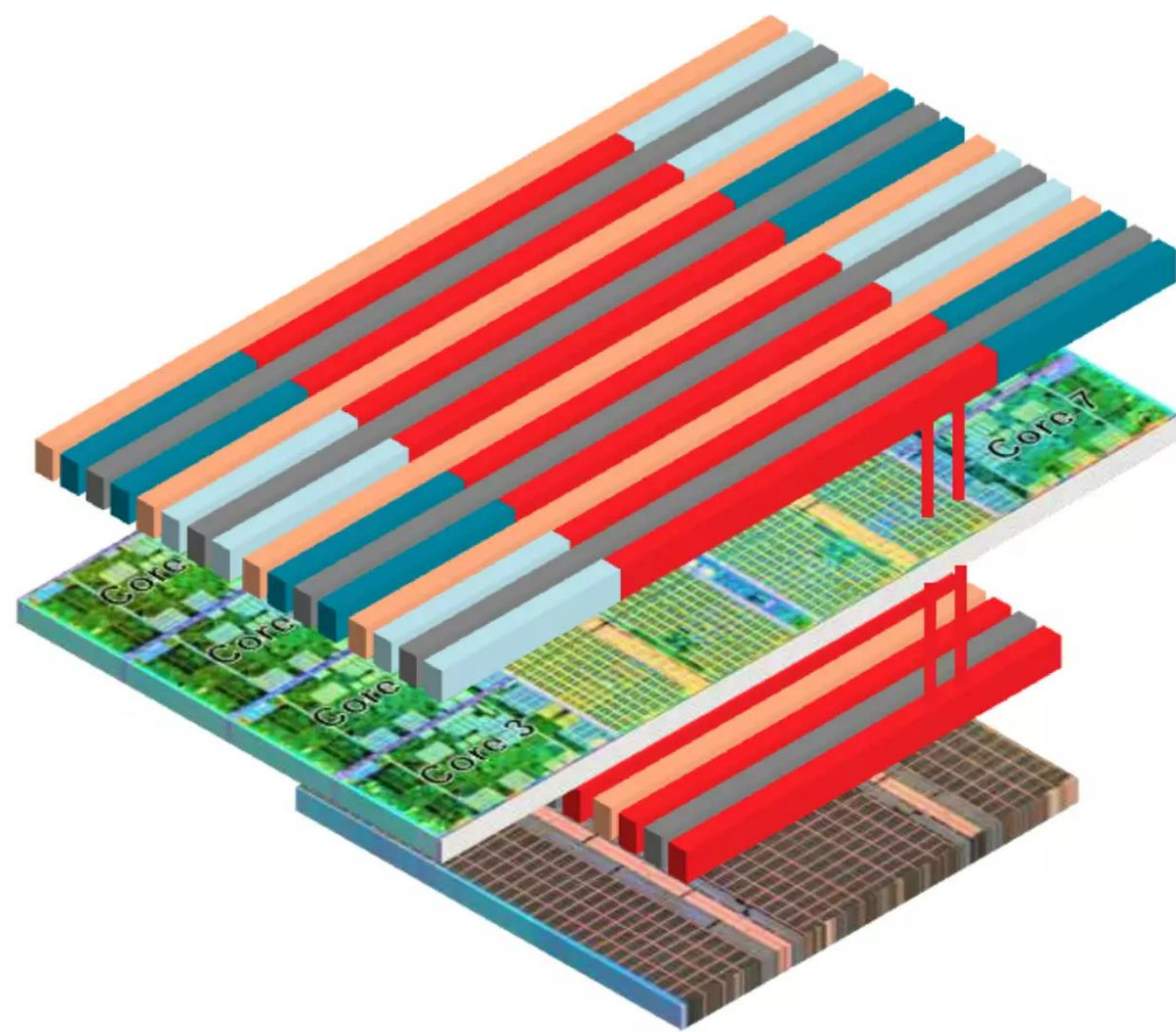


1. Objectives



Courtesy of AMD

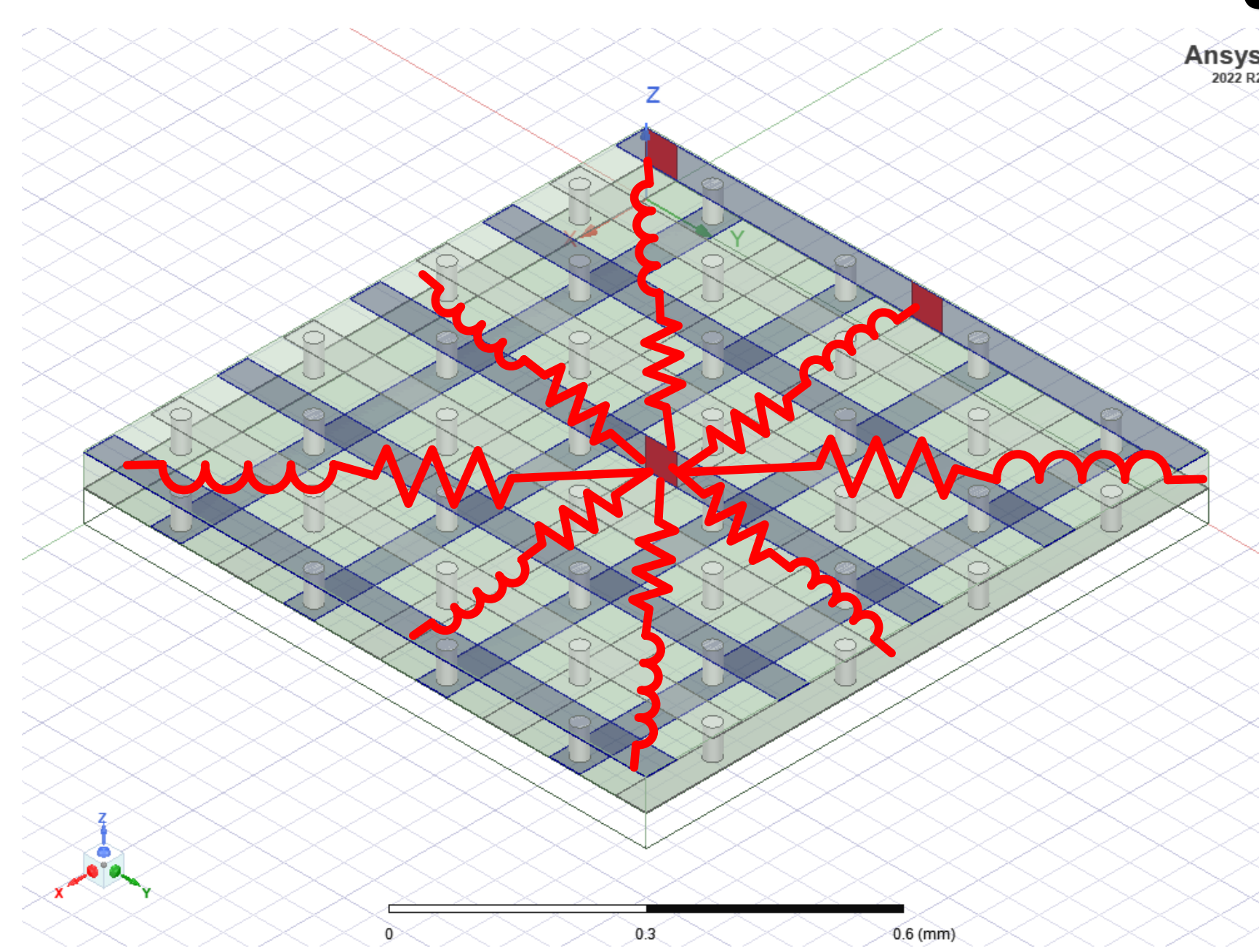
RVDD: Ungated supply
VDD: Per-core gated supply
VDDM: Gated L2/L3 SRAM supply



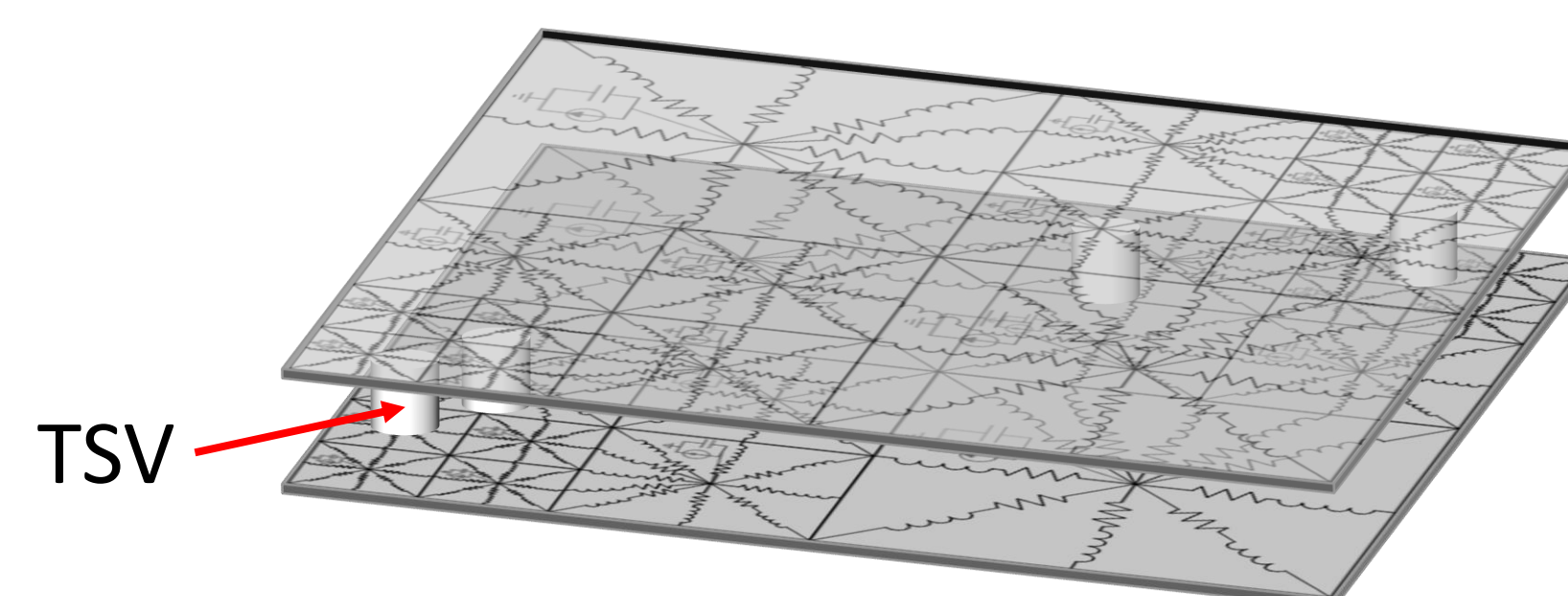
Courtesy of AMD

- Because of advances in machine learning and AI, demands on high-performance processing units are highly increased.
- On the other hand, development of the semiconductor technology has been gradually slowed down.
- The scaling of embedded memories in a processing unit is not as efficient as that of logic gates in technology development, and static power consumption of it is significantly increased.
- Therefore, 3-D chiplet architecture with different technology for each IPs are recently studied.
- In a 3-D chiplet, where more than two chips are stacked and share a power delivery network (PDN), analyzing the PDN becomes significantly complicated.
- We are developing equivalent model of on-chip + package PDN for efficient and accurate simulation

2. Power delivery network (PDN) modeling and through silicon via (TSV) optimization



Ansys
2022 02



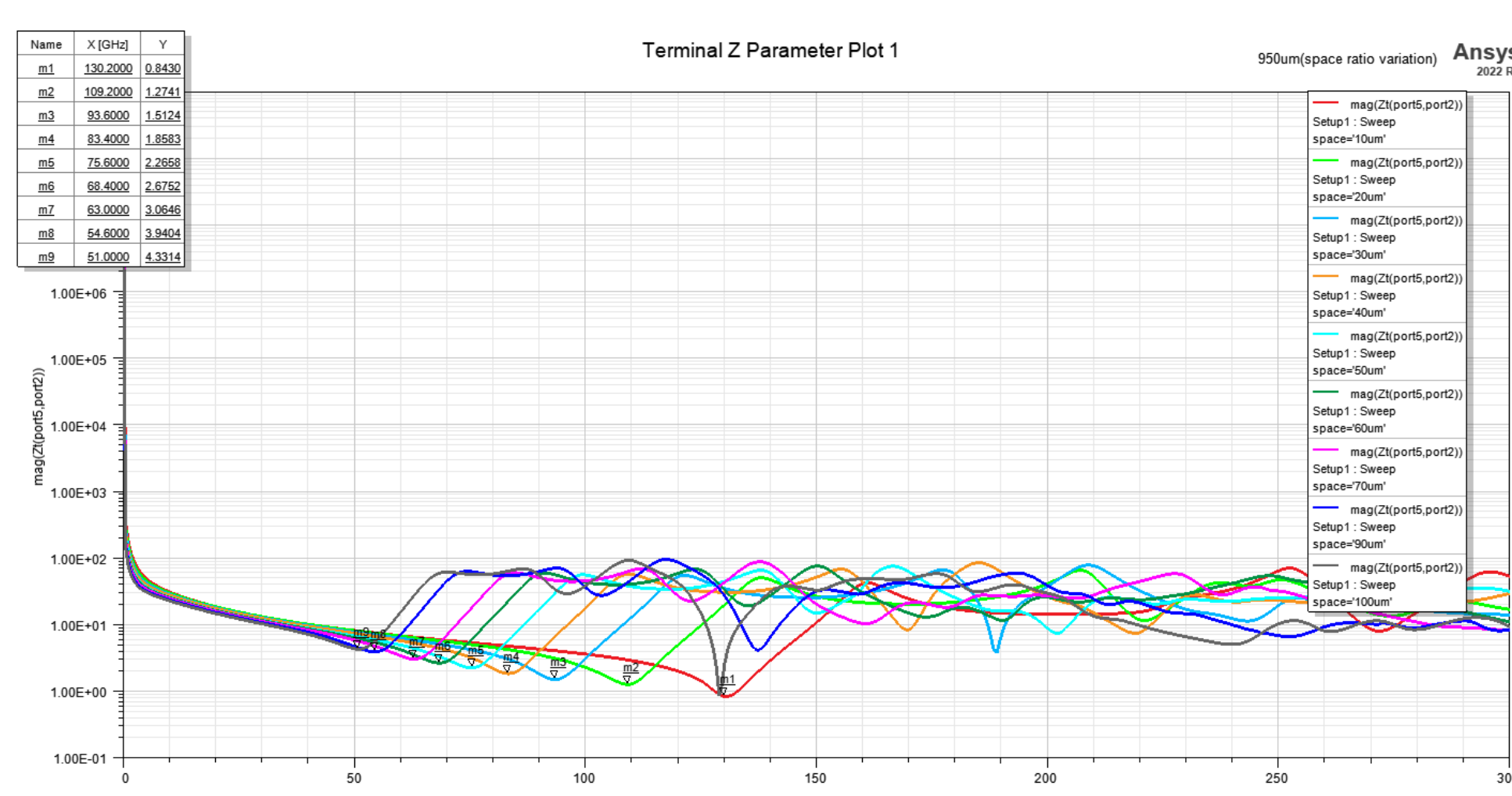
[Power delivery TSV optimization]

- We use the finite element analysis (FEA) simulator ANSYS to calculate inductance, as well as resistance and capacitance.

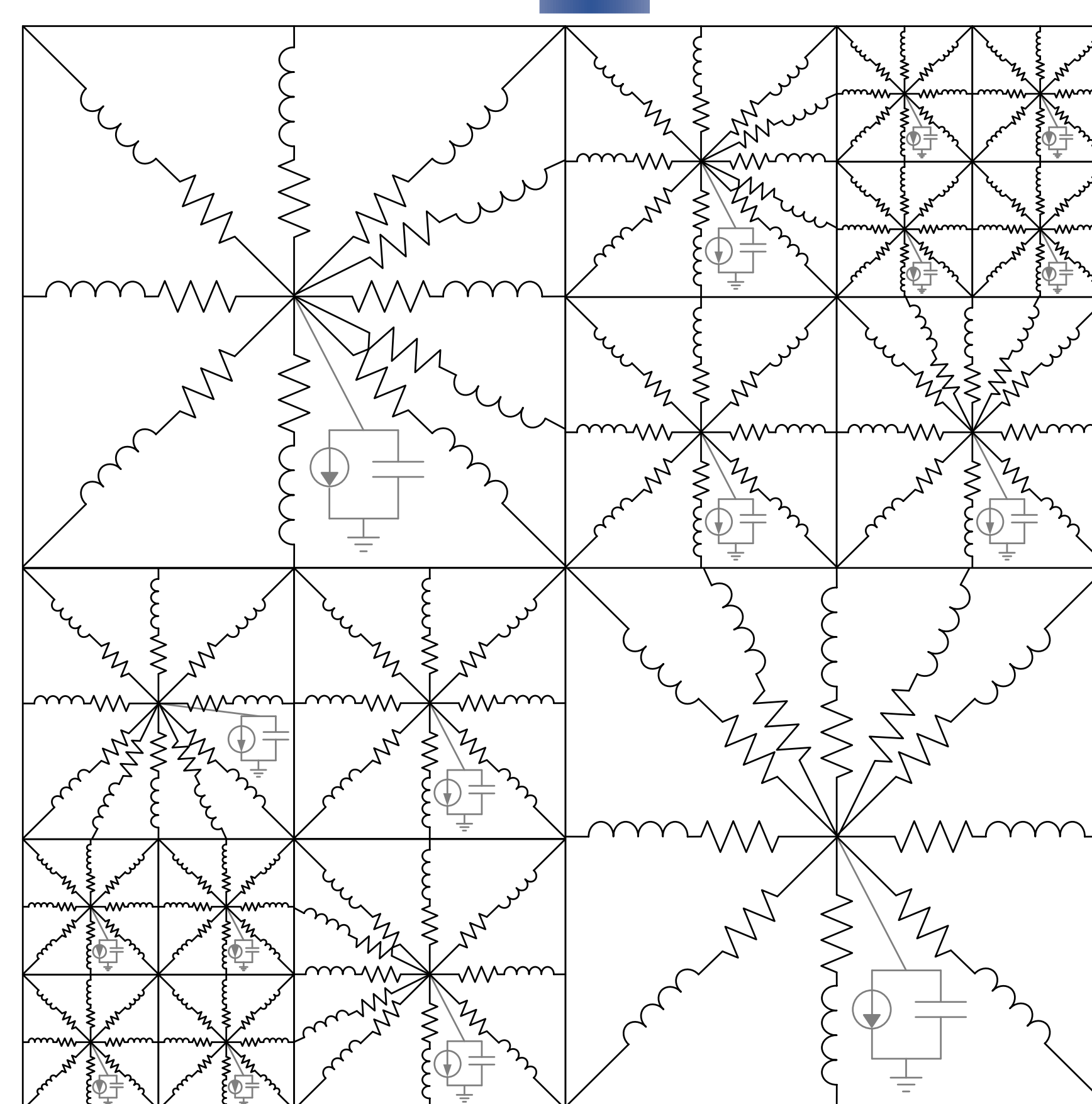
- Based on the S-parameter, we calculate Z-parameter and corresponding RLC values.

- To reduce the complexity of the power delivery network (PDN), we use small "tiles" for areas requiring detailed analysis, and larger "tiles" for other areas.

- We optimize the number and placement of TSVs for power delivery based on the analysis of the PDN.



[PDN simulation in FEA simulator]



[PDN equivalent modeling]

3. Collaboration with United states

- We are plan to collaborate with Professor Degertekin in GeorgiaTech about brain cancer immunotherapy.
- We are plan to collaborate with Professor Kiani in PennState university about packaging under wireless power transmission environment.



PennState

Georgia
Tech

